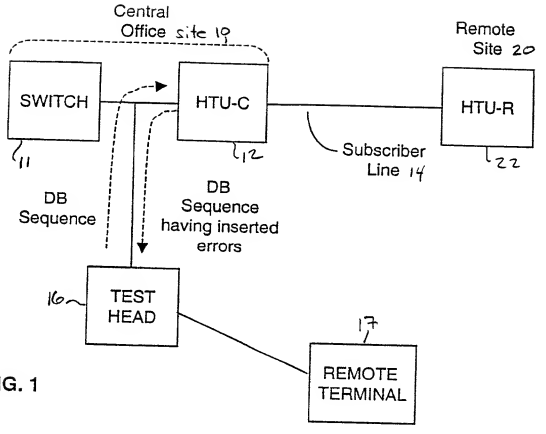

FIG. 1

If Margin is	and Pulse Attenuation is	then Bit Errors
5 or less	31 or higher	101
5 or less	26 - 30	102
5 or less	0 - 25	103
6 - 10	31 or higher	104
6 - 10	26 - 30	105
6 - 10	0 - 25	106
11 or higher	31 or higher	107
11 or higher	26 - 30	108
11 or higher	0 - 25	109

FIGURE 2

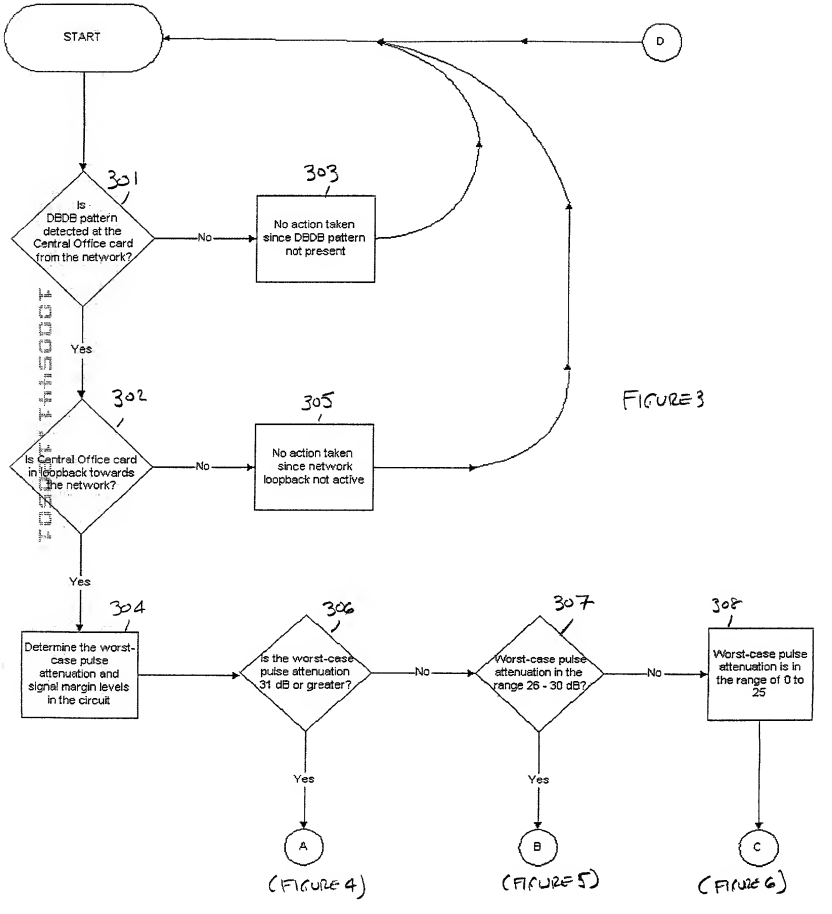
START
D
301
Is DBDB pattern detected at the Central Office card from the network?
No
303
No action taken since DBDB pattern not present
Yes
302
Is Central Office card in loopback towards the network?
No
305
No action taken since network loopback not active
Yes
304
Determine the worst-case pulse attenuation and signal margin levels in the circuit
306
Is the worst-case pulse attenuation 31 dB or greater?
No
307
Worst-case pulse attenuation in the range 26 - 30 dB?
No
308
Worst-case pulse attenuation is in the range of 0 to 25
Yes
Yes
Yes
A
B
C
(FIGURE 4)
(FIGURE 5)
(FIGURE 6)

FIGURE 3

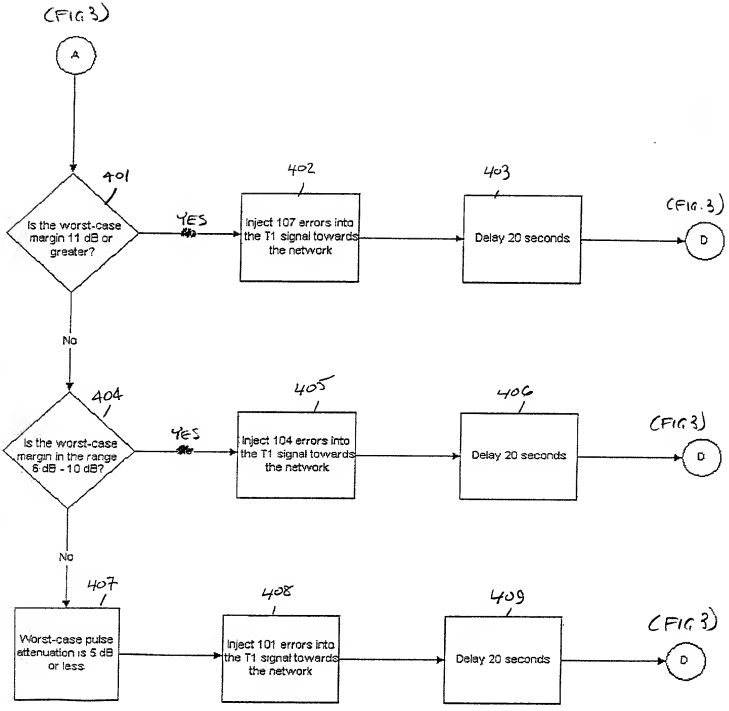
(FIG 3)
A
401
Is the worst-case margin 11 dB or greater?
YES
402
Inject 107 errors into the T1 signal towards the network
403
Delay 20 seconds
(FIG. 3)
D
No
404
Is the worst-case margin in the range 6 dB - 10 dB?
YES
405
Inject 104 errors into the T1 signal towards the network
406
Delay 20 seconds
(FIG 3)
D
No
407
Worst-case pulse attenuation is 5 dB or less
408
Inject 101 errors into the T1 signal towards the network
409
Delay 20 seconds
(FIG 3)
D

FIGURE 4

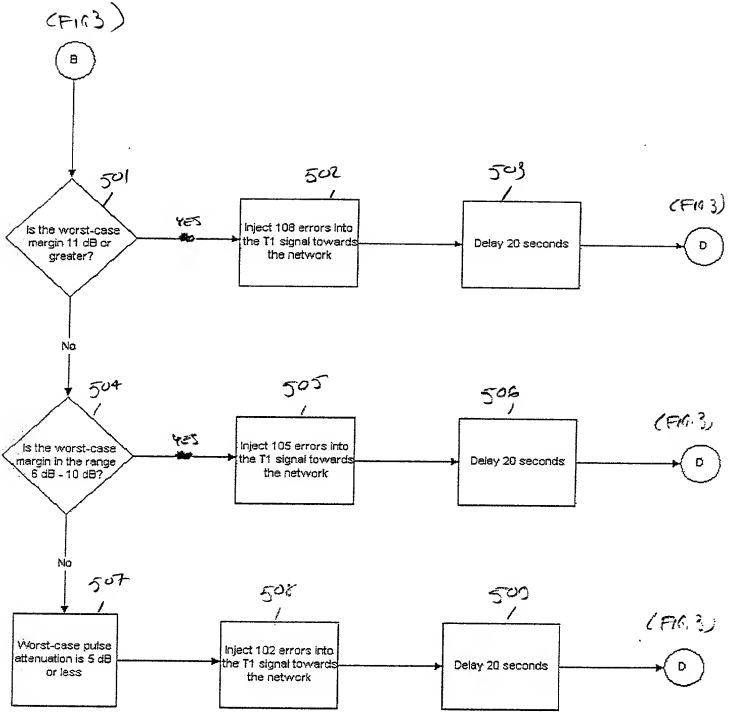
(FIG 3)
B
501
Is the worst-case margin 11 dB or greater?
YES
502
Inject 108 errors into the T1 signal towards the network
503
Delay 20 seconds
(FIG 3)
D
No
504
Is the worst-case margin in the range 6 dB - 10 dB?
YES
505
Inject 105 errors into the T1 signal towards the network
506
Delay 20 seconds
(FIG 3)
D
No
507
Worst-case pulse attenuation is 5 dB or less
508
Inject 102 errors into the T1 signal towards the network
509
Delay 20 seconds
(FIG 3)
D

FIGURE 5

FOR PATENT PURPOSES

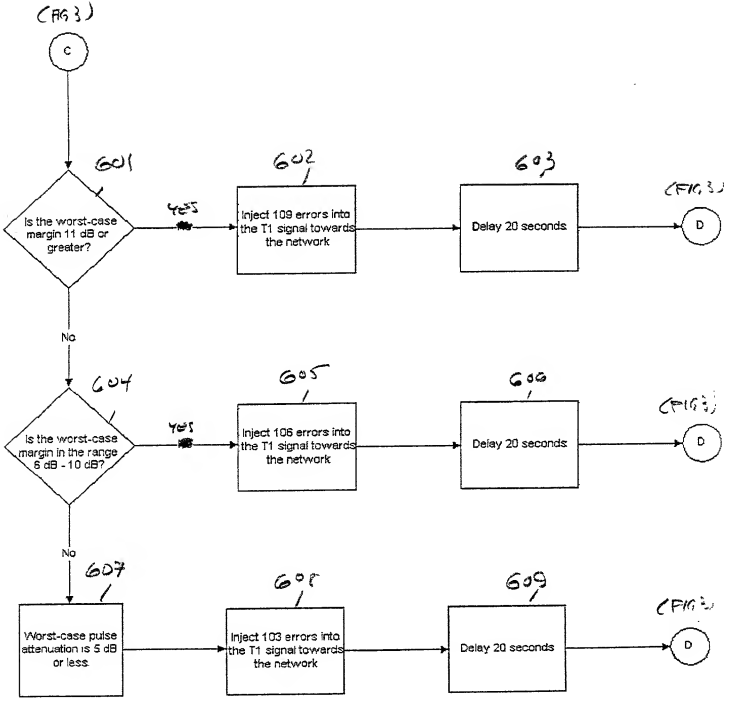

FIGURE-C